IN THE CLAIMS

Claim 1 (currently amended): A method for precluding stress-induced void formation in a semiconductor component, comprising:

providing a semiconductor substrate; ~~and~~

forming a first portion of a metallization system above the semiconductor substrate, the first portion ~~having a void preclusion feature~~ vertically spaced apart from the semiconductor substrate by a first distance, wherein forming the first portion includes:

forming a first layer of dielectric material over the semiconductor substrate;

forming a first opening in the first layer of dielectric material, the first opening having a surface, wherein at least one dielectric protrusion extends from the surface of the first opening;

forming a second opening in the first layer of dielectric material, the second opening having a surface, wherein at least one dielectric protrusion extends from the surface of the second opening; and

forming an electrically conductive material in the first and second openings; and

forming a second portion of the metallization system, the second portion coupled to the first portion and vertically spaced apart from the semiconductor substrate by a second distance, the second distance different from the first distance.

Claim 2 (canceled)

Claim 3 (currently amended): The method of claim 2, wherein forming the first and second openings ~~at least one opening~~ includes using an anisotropic reactive ion etch to form the first and second openings ~~at least one opening~~.

Claim 4 (currently amended): The method of claim ~~2~~ 1, wherein the at least one ~~portion of the~~ dielectric protrusion in the first opening and the at least one dielectric protrusion in the second opening have ~~material that remains adjacent the at least one opening has~~ a polygonal shape.

Claim 5 (original): The method of claim 4, wherein the polygonal shape is selected from the group of polygonal shapes consisting of a square, a rectangle, a pentagon, a triangle, a hexagon, a heptagon, and an octagon.

Claim 6 (currently amended): The method of claim ~~2~~ 1, wherein the at least one ~~portion of the~~ dielectric protrusions in the first and second openings have ~~material that remains adjacent the at least one opening has~~ a circular shape.

Claim 7 (canceled)

Claim 8 (currently amended): The method of claim ~~7~~ 1, ~~further including coupling the first portion of the metallization system to the second portion of the metallization system with a third portion of the metallization system,~~ wherein a width of the second ~~third~~ portion of the metallization system is less than a width of the first portion ~~and second portions~~ of the metallization system.

Claim 9 (canceled)

Claim 10 (currently amended): The method of claim ~~9~~ 1, wherein the second distance is less than the first distance.

Claim 11 (currently amended): A method for manufacturing a metallization system capable of precluding stress-induced void formation in a portion thereof, the method comprising:

providing a semiconductor substrate;

forming ~~disposing~~ a first portion of a conductive interconnect over the semiconductor substrate, the first portion having a width, wherein forming the first portion includes:

forming a first layer of dielectric material over the semiconductor substrate; and

forming a first trench in the first layer of dielectric material, the first trench having at least one dielectric pillar;

forming a second portion of the conductive interconnect over the semiconductor substrate, the second portion having a width, wherein forming the second portion includes:

forming a second trench in the first layer of dielectric material, the second trench having at least one dielectric pillar, wherein the first and second trenches are laterally spaced apart from each other; and

disposing a second electrically conductive material in the first and second trenches;

forming a third portion of the conductive interconnect over the semiconductor substrate, wherein the third portion is coupled between the first portion and the second portions of the conductive interconnect.~~; and~~

~~forming a plurality of apertures in the first portion of the conductive interconnect.~~

Claim 12 (canceled)

Claim 13 (currently amended): The method of claim 11, wherein forming the ~~disposing the first, second, and~~ third portion ~~portions~~ of the conductive interconnect comprises:

forming ~~disposing~~ a ~~first~~ second layer of dielectric material over the semiconductor substrate, the second layer of dielectric material between the semiconductor substrate and the first layer of dielectric material;

forming at least one ~~a~~ trench in the ~~first~~ second layer of dielectric material; and

disposing a third ~~filling the trench with~~ electrically conductive material in the at least one trench in the second layer of dielectric material to form a filled trench that serves as the third portion of the conductive interconnect~~;~~

~~disposing a second layer of dielectric material over the filled trench;~~

~~forming a plurality of openings in the second layer of dielectric material, a first opening exposing a first portion of the filled trench and a second opening exposing a second portion of the filled trench; and~~

~~filling the plurality of openings with additional electrically conductive material, wherein electrically conductive material filling a first opening of the plurality of openings serves as the first portion of the conductive interconnect and the electrically conductive material filling a second opening of the plurality of openings serves as the second portion of the conductive interconnect~~.

Claim 14 (currently amended): A ~~The~~ method for manufacturing a metallization system capable of precluding stress-induced void formation in a portion thereof, the method comprising: ~~of claim 11~~

providing a semiconductor substrate;

disposing a first portion of a conductive interconnect over the semiconductor substrate, the first portion having a width;

disposing second and third portions of the conductive interconnect over the semiconductor substrate, the first and second portions vertically spaced apart from the semiconductor substrate by a first distance and laterally spaced apart from each other, and the third portion vertically spaced apart from the semiconductor substrate by a second distance, the second distance different from the first distance, wherein disposing the first, second, and third portions of the conductive interconnect comprises:

disposing a first layer of dielectric material over the semiconductor substrate;

forming first and second trenches in the first layer of dielectric material, the first and second trenches having dielectric pillars formed therein;

filling the first and second trenches with electrically conductive material to form the first and second portions of the conductive interconnect;

disposing a second layer of dielectric material over the first and second portions of the conductive interconnect;

forming a third trench, the third trench in the second layer of dielectric material;

forming first and second vias in the second layer of dielectric material, the first via exposing the first portion of the conductive interconnect and the second via exposing the second portion of the conductive interconnect; and

filling the third trench and the first and second vias with an electrically conductive material, wherein the electrically conductive material filling the first via electrically couples the first portion of the conductive interconnect to the third portion of the conductive interconnect and the electrically conductive material filling the second via couples the second portion of the conductive interconnect to the third portion of the conductive interconnect.

Claim 15 (original): The method of claim 14, wherein forming the dielectric pillars includes forming square shaped dielectric pillars.

Claim 16 (currently amended): The method of claim 11, wherein ~~forming the first, second, and third portions~~ forming the third portion of the conductive interconnect includes:

forming a ~~first~~ second layer of dielectric material over the semiconductor substrate, wherein the first layer of dielectric material is between the semiconductor substrate and the second layer of dielectric material;

~~disposing an electrically conductive material over the layer of dielectric material;~~

~~forming the first and second portions of the conductive interconnect from the electrically conductive material;~~

forming at least one opening in the ~~each of the first and second portions of the conductive interconnect;~~

~~forming a~~ second layer of dielectric material ~~over the first and second portions of the conductive interconnect~~;

~~forming first and second openings in the second layer of dielectric material, the first opening exposing the first portion of the conductive interconnect and the second opening exposing the second portion of the conductive interconnect; and~~

disposing ~~additional~~ a second electrically conductive material ~~over~~ in the at least one opening in the second layer of dielectric material to form a filled opening that serves as the third portion of the conductive interconnect~~, the second layer of electrically conductive material filling the first and second openings in the second layer of dielectric material~~.

Claims 17-22 (canceled)

Claim 23 (new): The method of claim 1, wherein the step of forming the second portion of the metallization system comprises:

forming a second layer of dielectric material over the semiconductor substrate, the second layer of dielectric material disposed between the first layer of dielectric material and the semiconductor substrate;

forming at least one opening in the second layer of dielectric material; and

forming an electrically conductive material in the at least one opening in the second layer of dielectric material, wherein the electrically conductive material in the at least one opening in the second layer of dielectric material is electrically coupled to the first electrically conductive material.

Claim 24 (new): The method of claim 1, wherein the step of forming the second portion of the metallization system comprises:

forming a second layer of dielectric material over the semiconductor substrate, wherein the first layer of dielectric material is disposed between the second layer of dielectric material and the semiconductor substrate;

forming at least one opening in the second layer of dielectric material; and

forming a second electrically conductive material in the at least one opening in the second layer of dielectric material, wherein the second electrically conductive material in the at least one opening in the second layer of dielectric material is electrically coupled to the first electrically conductive material.

Claim 25 (new): The method of claim 11, wherein forming the first trench includes forming the at least one dielectric pillar in the first trench having a polygonal shape and wherein forming the second trench includes forming the at least one dielectric pillar in the second trench having a polygonal shape.

Claim 26 (new): The method of claim 11, wherein forming the third portion of the conductive interconnect includes:

forming a second layer of dielectric material over the semiconductor substrate;

forming trench in the second layer of dielectric material; and

disposing a third electrically conductive material in the trench in the second layer of dielectric material.

Claim 27 (new): The method of claim 26, wherein the second layer of dielectric material is between the first layer of dielectric material and the semiconductor substrate.

Claim 28 (new): The method of claim 26, wherein the first layer of dielectric material is between the second layer of dielectric material and the semiconductor substrate.